# PATENT SPECIFICATION (11) 1427014

1427014

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## (54) SEMICONDUCTOR DEVICES


(71) We, SONY CORPORATION, a corporation organized and existing under the laws of Japan of 7—35 Kitashinagawa-6, Shinagawa-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—


This invention relates to semiconductor devices.

According to the present invention there is provided a semiconductor device comprising:

a substrate of semiconductor material of one conductivity type having first and second opposed surfaces;

a first region of the opposite conductivity type on the first surface of the substrate forming a first pn junction therewith;

a second region of said opposite conductivity type on or adjacent to the first surface of the substrate forming a second pn junction therewith which surrounds said first junction in predetermined spaced relation; and

a third region of said opposite conductivity type on or adjacent to the second surface of the substrate forming a third pn junction therewith which faces said first region in predetermined spaced relation therewith;

said second and third regions being free of electrical connection; and

the arrangement being such that the depletion layer associated in use with said first junction reaches said second and third junctions at a biasing potential across said first junction which is lower than that at which said first junction would, in the absence of said second and third junctions, break down.

Embodiments of the invention can be made in planar form and have a much higher reverse breakdown voltage characteristic than has previously been possible.

The invention will now be described by way of example with reference to the accompanying drawings, in which:—

Figure 1 diagrammatically illustrates a prior art type of planar diode;

Figure 2 is a fragmentary sectional view of a planar-type junction device forming an embodiment of the present invention;

Figure 3 is a diagram of the current-voltage characteristic of the device of Figure 2;

Figure 4 diagrammaticaly shows a planar-type transistor embodiment;

Figure 5 is a view similar to Figure 4, but showing a modification thereof; and

Figures 6 to 9 are diagrammatic views of other embodiments, these embodiments being respectively a transistor, a gate controlled switch, a transistor and a gate controlled switch.

Figure 1 of the drawings illustrates a prior art form of device such as that described in US Patent Specification No. 3,555,878. Specifically there is shown in Figure 1, a planar-type diode having a substrate 3 of semi-conductor material with n-type impurity. Diffused into the upper surface of the substrate 3 is a p-type region 4 which forms a pn junction 5 with the substrate 3. It will be understood that the region 4 forms the anode and the substrate 3 the cathode of the diode. An anode electrode 9 is formed in contact with the region 4, while an ohmic contact 10 is provided on the under surface of the substrate 3. A guard ring 6 of p-type material is also diffused into the upper surface of the substrate 3 around the main region 4. There is no electrical connection to this guard ring 6, but it will be appreciated that a pn junction 5′ formed between the guard ring 6 and the substrate 3. An oxide coating 8 is preferably provided on the upper surface of the device, except the portion covered with the anode 9.

When a negative voltage is applied to the diffused region 4, the depletion layer 7 extends from the region 4 and reaches the guard ring 6 at a voltage which is lower than the breakdown voltage of the main pn junction 5. When a guard ring is provided for a planar device, the reverse voltage breakdown characteristic is improved because the curvature of the pn junction is moderated by the guard ring.

The device of Figure 1 is inferior to a mesa-type device having a flat junction, inso-

far as its reverse volatge breakdown characteristic is concerned. Thus the potential $E_a$ at an arbitrary point A (in Figure 1) is a composite of the potential $E_{po}$ due to the diffusion region 4, and the potential $E_{pl}$ due to the guard ring 6. As the voltage applied to the diffusion region 4 increases, the potential difference between the region 4 and the ring 6 increases, and finally the device breaks down before the surface portion of the pn junction 5 breaks down.

One preferred embodiment of the present invention is shown in Figure 2. Here a substrate 11 of silicon with n-type impurity has diffused in the upper surface thereof a main region 12 of p-type impurity and a plurality of guard rings 14*a*, 14*b* and 14*c* of p-type impurity spaced therearound. An auxiliary region 12′ of p-type impurity is diffused in the opposite surface of the substrate 11. This auxiliary region 12′ is of larger diameter than the main region 12 for reasons which will hereinafter be made apparent. Also diffused into the lower surface of the substrate 11, are a plurality of guard rings of p-type impurity, 14*a*′, 14*b*′ and 14*c*′. These guard rings are spaced slightly laterally outwardly from the corresponding guard rings 14*a*, 14*b* and 14*c* formed in the upper surface of the substrate 11.

An anode electrode 15 is provided on the main region 12 and a cathode electrode 24 is provided as shown in Figure 2, which connects to the substrate 11 through a high impurity concentration n+ region 19. This is provided for making an appropriate ohmic contact of the electrode 24 with the substrate 11.

The distance between the main region 12 and the guard rings 14*a* to 14*c* are selected to be predetermined values. The distance between the region 12 and the region 12′ has also a predetermined value. As will be apparent from an inspection, the auxiliary region 12′ is designed to have its edge portion offset with respect to the main region 12 (that is the reason auxiliary region 12′ is larger than the main region 12). The auxiliary guard ring 14*a*′ is offset with respect to the corresponding guard ring 14*a*. Similarly, the auxiliary guard rings 14*b*′ and 14*c*′ are offset with respect to the corresponding guard rings 14*b* and 14*c* respectively.

A depletion layer 20 will extend from the main region 12 and the guard ring 14*a*, and will reach the auxiliary region 12′ before the pn junction 13 breaks down. The potential at point A in Figure 2 is a composite of three potentials, $E_{po}$ due to the main region 12, $E_{pl}$ due to the guard ring 14*a*, and $E_{p'o}$ due to the auxiliary region 12′. The composite potential is relatively small because the potential $E_{p'o}$ due to the auxiliary region 12′ is directed upwardly, by reason that the auxiliary region 12′ is larger than the main region 12. Thus, the depetion layer 20 will expand from the main region 12 to the guard rings 14*a* to 14*c* and to the auxiliary guard rings 14*a*′ to 14*c*′, hence the overall breakdown voltage becomes extremely high as is desired. The total breakdown voltage $V_B$ is given by:

$$V_B = nV_p + V$$

where:

$V_p$ is the punch-through voltage between the main region 12 and the guard ring 14*a* or between the nearest guard rings: V is the breakdown voltage of the outermost guard ring; and $n$ is the number of guard rings.

By way of example, a device of this type might have the following physical dimensions:

n=15;
diffusion depth $X_j$ of p-type impurity into the substrate 11=30 microns;
thickness of the substrate 11=200 microns with a resistivity of 120 ohm-cm.;
the distance W between the guard rings and between the main region 12 and the guard ring 14*a*=130 microns.

With a construction having these characteristics and dimensions, the device of Figure 2 will have the characteristic as shown in Figure 3. Here the breakdown voltage is about 7 kilovolts, which is superior to that of a conventional mesa-type device (the conventional mesa-type device usually being about 3 kilovolts).

Figure 4 illustrates a planar-type transistor. In Figure 4 reference numerals similar to those of Figure 2 indicate similar elements. Here the emitter is provided by an n+ diffused region 13′ which has been diffused into a p-type diffused base region 12, which in turn has been diffused into the n-type substrate 11 to form a pn junction jc therebetween. The substrate 11, of course, forms the collector. A guard ring 14*a* of p-type impurity is provided in the upper surface and is so formed that the depletion layer 18 will reach the guard ring 14*a* first, and then reach the auxiliary region 16 of p-type which has been diffused into the opposite surface of the substrate 11. An additional guard ring 14*b* of p-type impurity is formed to surround the guard ring 14*a* in the upper surface, and two further guard rings 15*a* and 15*b* of p-type are provided to surround the guard ring 14*b*. Guard ring 14*a* is relatively close to the region 12, this distance being specified in Figure 4 as $L_1$. Guard ring 14*b* is separated from guard ring 14*a* by a similar distance $L_2$. Guard ring 15*a* is separated from guard ring 14*b* by a much greater distance $W_1$ than the distance $L_1$ and

$L_2$. Guard ring 15*b* is also spaced from guard ring 15*a* by a distance $W_2$ as shown in the drawing. The depletion regions are shown by the broken lines in Figure 4. The structure of Figure 4 has an n+ diffused region 19 to facilitate an ohmic contact through electrode 24 to the substrate 11. The emitter region 13′ is provided with an electrode 25, as shown, and the base region 12 is also provided with an electrode 26, as shown. There are no electrodes to the auxiliary region 16, or to any of the guard rings. An oxide coating 27 is provided on the upper surface of the device, and an oxide coating 28 is provided on the lower surface of the device. Auxiliary guard rings 17*a* and 17*b* of p-type are formed in the lower sufrace of the substrate 11 to surround the auxiliary region 16.

Figure 5 shows a variation of the structure shown in Figure 4. Here the auxiliary region 16 and the auxiliary guard rings 17*a* and 17*b* are embedded in the substrate 11. The inner guard rings 14*a* and 14*b* surrounding the base region 12 are also embedded, as shown. The other features of Figure 5 are substantially the same as those of Figure 4, so no further description will be given.

Figure 6 shows a transistor with guard rings 14*a* and 14*b* of p-type impurity formed in an n-type substrate 11, generally similar to the structure shown in Figure 4. Here, however, there is an intermediate region 116 of p-type impurity embedded in the substrate 11 between the region 12 and the region 16 but spaced therefrom. This readily extends the depletion layer from the base region 12 to the region 16. In the example of Figure 6, the guard rings 15*a* and 15*b* used in Figure 4 are dispensed with.

Figure 7 shows a device somewhat similar to Figure 6, but in this case the device is a gate controlled switch. The device includes the same guard rings as in Figure 6, and the same intermediate region 116. In this example a p-type region 34 is formed in the substrate 11 and an electrode 34′ is formed thereon.

Figure 8 shows a transistor, the base region 12 of which includes a main portion 12*a* immediately below the emitter 13′ and a downwardly extending peripheral portion 12*b*. This further enables the depletion layer readily to extend downwardly to the auxiliary region 16, and makes the base-transport factor sufficiently high. The auxiliary region 16 has two guard rings 17*a* and 17*b* surrounding it. Two guard rings 14*a* and 14*b* surround the base region 12 in the manner and for the reasons hereinabove described in connection with previous embodiments. Oxide coatings 27 and 28 are provided on the upper and lower surfaces of the device. Emitter electrode 25 is provided for the emitter region 13′, while a base electrode 26 is provided for the base region 12. The collector region is provided with an electrode 24 which connnects to the collector region through an n+ impurity region 29.

Figure 9 is similar to Figure 8, except that it is a gate controlled switch as distinct from a transistor. This will be apparent from an inspection of the arrangement of the electrodes.

In view of Section 9 of the Patents Act, 1949, attention is drawn to our Patent No. 1,078,273.

## WHAT WE CLAIM IS:—

1. A semiconductor device comprising:

a substrate of semiconductor material of one conductivity type having first and second opposed surfaces;

a first region of the opposite conductivity type on the first surface of the substrate forming a first pn junction therewith:

a second region of said opposite conductivity type on or adjacent to the first surface of the substrate forming a second pn junction therewith which surrounds said first junction in predetermined spaced relation; and

a third region of said opposite conductivity type on or adjacent to the second surface of the substrate forming a third pn junction therewith which faces said first region in predetermined spaced relation therewith;

said second and third regions being free of electrical connection; and

the arrangement being such that the depletion layer associated in use with said first junction reaches said second and third junctions at a biasing potential across said first junction which is lower than that at which said first junction would, in the absence of said second and third junctions, break down.

2. A device according to claim 1 wherein said third region is larger than said first region.

3. A device according to claim 1 or claim 2 wherein said second region has a larger outside periphery than that of said third region.

4. A device according to claim 1, claim 2 or claim 3 wherein a fourth region of said opposite conductivity type is formed on or adjacent to said second surface of said substrate forming a fourth pn junction therewith which surrounds said third pn junction in predetermined spaced relation thereto.

5. A device according to claim 4 comprising a plurality of said second regions and a plurality of said fourth regions respectively surrounding said first junction and said third junction.

6. A device according to any one of the preceding claims comprising an intermediate region of the opposite conductivity type located between said first and third regions.

7. A planar device according to any one of the preceding claims.

8. A semiconductor device substantially as described with reference to Figure 2 of the accompanying drawings.

9. A semiconductor device substantially as described with reference to Figure 4 of the accompanying drawings.

10. A semiconductor device substantially as described with reference to Figure 5 of the accompanying drawings.

11. A semiconductor device substantially as described with reference to Figure 6 of the accompanying drawings.

12. A semiconductor device substantially as described with reference to Figure 7 of the accompanying drawings.

13. A semiconductor device substantially as described with reference to Figure 8 of the accompanying drawings.

14. A semiconductor device substantially as described with reference to Figure 9 of the accompanying drawings.

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3 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG.1.
PRIOR ART

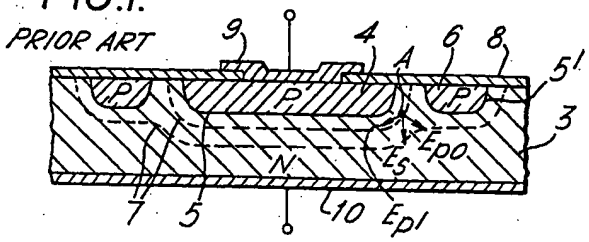



FIG.2.

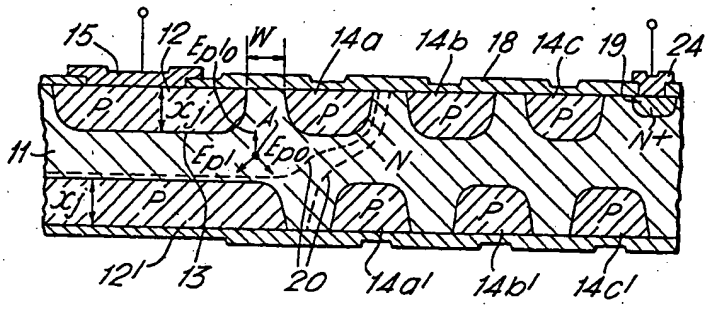



FIG.3.

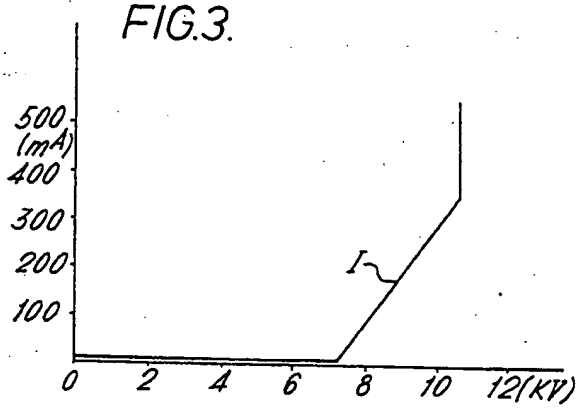


FIG.4.

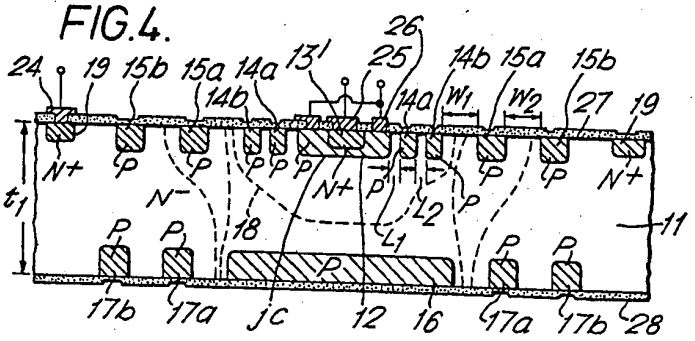



FIG.5.

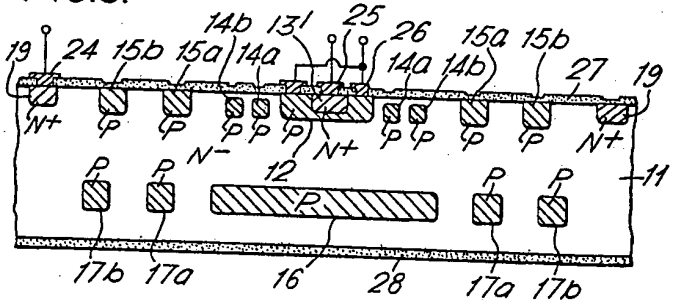
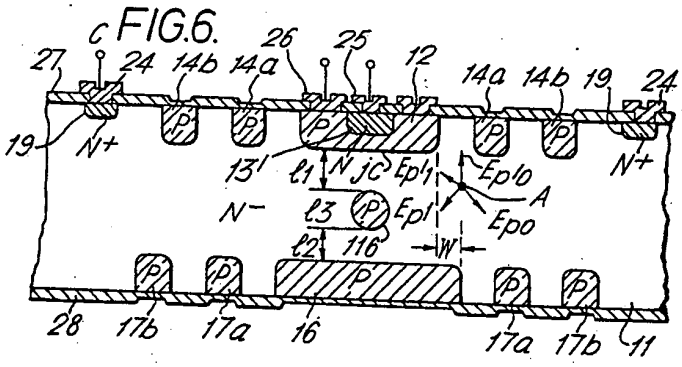



FIG.6.



1427014 COMPLETE SPECIFICATION
3 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 3

FIG.7.

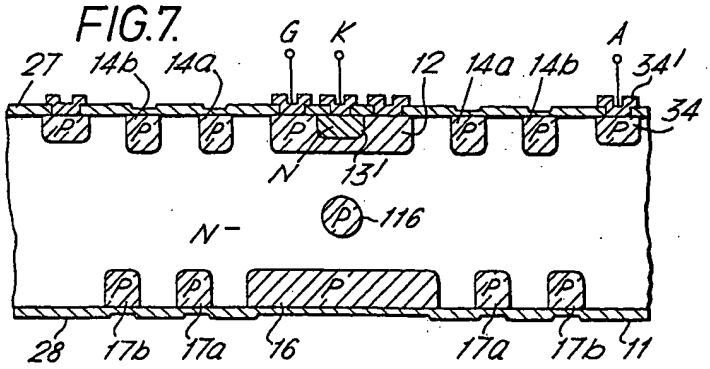



FIG.8.

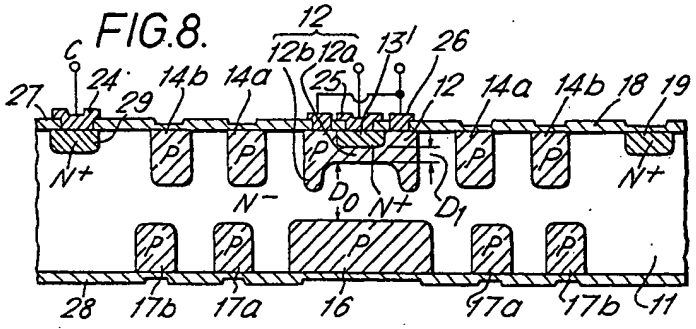



FIG.9.